**What is claimed is:**

1. An array substrate for a liquid crystal display device, comprising:

a substrate;

gate and data lines crossing each other on the substrate;

a thin film transistor connected to the gate and data lines, the thin film transistor having a semiconductor layer, and source and drain electrodes facing and spaced apart from each other;

a passivation layer over the gate and data lines and the thin film transistor, the passivation layer having a contact hole exposing a portion of a side surface of the drain electrode; and

a pixel electrode on the passivation layer.

2. The array substrate according to claim 1, wherein the pixel electrode is electrically connected to the drain electrode through the contact hole.

3. The array substrate according to claim 1, wherein the semiconductor layer has the same plane surface as the data line and the source and drain electrodes except for a portion between the source and drain electrodes.

4. The array substrate according to claim 1, further comprising:

a gate insulation layer formed underneath the passivation layer, wherein the contact hole is defined through the passivation layer and the gate insulation layer.

5. The array substrate according to claim 1, wherein the contact hole further exposes a portion of a top surface of the drain electrode.

6. An array substrate for a liquid crystal display device, comprising:

a substrate;

gate and data lines crossing each other on the substrate;

a thin film transistor connected to the gate and data lines, the thin film transistor having a semiconductor layer, a plurality of ohmic contact layers, and source and drain electrodes;

a passivation layer pattern on the data line and the thin film transistor, the passivation layer pattern exposing a portion of a side surfaces of the drain electrode; and

a pixel electrode connected to the drain electrode.

7. The array substrate according to claim 6, wherein the semiconductor layer has the same plane surface as the data line and the source and drain electrodes except for a portion of the semiconductor layer between the source and drain electrodes.

8. The array substrate according to claim 6, wherein the plurality of ohmic contact layers have the same plane surfaces as the data line and the source and drain electrodes.

9. The array substrate according to claim 6, wherein the passivation layer pattern exposes a portion of one side surface of the drain electrode.

10. The array substrate according to claim 6, further comprising:

a gate insulation film formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film.

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11. The array substrate according to claim 6, wherein the passivation layer pattern further exposes a portion of a top surface of the drain electrode.

12. An array substrate for a display device, comprising:

a substrate;

a gate line on the substrate;

a gate insulator on the gate line;

a semiconductor layer on the gate insulator;

a plurality of ohmic contact layers on the semiconductor layer;

a data line and source and drain electrodes on the plurality of ohmic contact layers, the source electrode connected to the data line, the drain electrode facing and spaced apart from the source electrode;

a passivation layer on the source and drain electrodes and covering a crossing portion of the gate and data lines, a portion of a side surface of the drain electrodes being exposed; and

a pixel electrode connected to the drain electrode,

wherein the plurality of ohmic contact layers have the same plane surfaces as the data line, and the source and drain electrodes, and

wherein the semiconductor layer has the same plane surface as the data line, and the source and drain electrodes except for a portion between the source and drain electrodes.

13. The array substrate according to claim 12, wherein a portion of the pixel electrode is formed directly on the gate insulator.

14. The array substrate according to claim 12, wherein the passivation exposes a portion of a top surface of the drain electrode.

15. A fabricating method of an array substrate for a liquid crystal display device, comprising:

forming a gate line on a substrate;

forming an ohmic contact layer on the substrate;

forming a data line and source and drain electrodes on the ohmic contact layer, the source electrode being connected to the data line, the source and drain electrodes facing and spaced apart from each other;

forming a passivation layer having a contact hole on the data line and the source and drain electrodes, the contact hole exposing a portion of a side surface of the drain electrode; and

forming a pixel electrode on the passivation layer, the pixel electrode being connected to the drain electrode through the contact hole.

16. The fabricating method according to claim 15, wherein the ohmic contact layer, the data line, and the source and drain electrodes are formed using a single mask.

17. The fabricating method according to claim 15, wherein the contact hole exposes a portion of a top surface of the drain electrode.

18. The fabricating method according to claim 15, further comprising:

forming a gate insulator on the gate line and under the passivation layer, wherein the contact hole is defined through the passivation layer and the gate insulator.

19. A fabricating method of an array substrate for a liquid crystal display device, comprising:

forming a gate line on a substrate using a first mask;

subsequently depositing a gate insulator, an amorphous silicon layer, a doped amorphous silicon layer and a conductive layer on the gate line;

forming a semiconductor layer, a plurality of ohmic contact layers, a data line, and source and drain electrodes using a second mask;

forming a passivation layer pattern on the source and drain electrodes using a third mask, the passivation layer pattern covering a crossing portion of the gate and the data lines and exposing a portion of a side surface of the drain electrode; and

forming a pixel electrode connected to the drain electrode using a fourth mask.

20. The fabricating method according to claim 19, wherein the passivation layer pattern further exposes a portion of a top surface of the drain electrode.

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21. The fabricating method according to claim 19, further comprising:

forming a gate insulator over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulator.